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10/608,085	06/30/2003	Yong-Sup Hwang	8733.873.00-US	8100

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EXAMINER	
SCHECHTER, ANDREW M	
ART UNIT	PAPER NUMBER
2871	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/608,085	HWANG ET AL.	
	Examiner	Art Unit	
	ANDREW SCHECHTER	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,9-12,14,15,17-20,25-28,30 and 31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9-12,14,15,17-20,25-28,30 and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 24 April 2008 have been fully considered but they are not persuasive. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

The applicant has amended independent claims 1 and 17 with the limitation of previous dependent claims 13 and 29 that there is a buffer layer between the substrate and the first barrier metal layer. This does not patentably distinguish the claims, as such a feature has already been held by the examiner to have been obvious in view of the teaching of such a buffer layer by *Terakado*, for instance. The previous rejection of the independent claims is therefore modified to include this teaching of *Terakado*.

The applicant has amended independent claims 1 and 17 to recite that each of the first and second barrier metal layers includes a metallic material which is either Ta and Ti. The previous claims 6 and 22 had limited the metallic material to one of Ta, Ti, Cr, Mo, Ni, W, and an alloy thereof – basically high melting point metals with good adhesion properties. The prior art cited in the previous rejection (*Kim* in view of *Jo*) does tend to single out Mo in particular, so this amendment restricting the list to Ta and Ti does somewhat distinguish over the previous rejection. However, it does not make the claims patentably distinct. First, *Jo* does in fact refer to using either Cu on Ti or Cu on Mo [see paragraph 0013]; although *Jo* then singles out Cu on Mo in particular, it is never made explicit why Mo is preferable to Ti, if indeed it is. Second, the prior art for

such multi-layer electrodes evidences that these metals are art-recognized equivalents for the purpose. For instance, U.S. Patent No. 5,650,834 to *Nakagawa et al.* discloses the use of a double layer with Al, Ag, or Cu on top and Cr, Mo, Ta, W, or Ni on bottom [col. 4, lines 61-65, for instance]. U.S. Patent No. 6,674,495 to *Hong et al.* teaches using Al, Ag, or Cu for their low resistivity and Cr, Mo, or Ti for their good contact properties [col. 10, lines 20-24, for instance]. U.S. Patent No. 6,184,964 to *Kameyama et al.* teaches a triple-layer with the lowest layer Ti, Cr, Mo, W, Al, Ta, or Ni for their adhesion properties and the second layer Cu or Ag for their low resistivity [see abstract, for instance]. From these prior art references, it can be seen that the use of Ta or Ti in place of Mo (as singled out by *Jo*, setting aside *Jo's* mentions of Ti) would have been obvious to one of ordinary skill in the art as a matter of being art-recognized equivalents for the known purpose of providing good adhesion properties while the Cu layer provides low electrical resistance. The following rejections are therefore appropriate.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4, 11, 12, 14, 15, 17-20, 27, 28, 30, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Kim,* U.S. Patent No. 6,043,511 in view of *Jo et al.,* US 2002/0081847, in view of *Onisawa et al.,* U.S. Patent No. 5,739,877, in view

of *Terakado et al.*, U.S. Patent No. 6,674,502, and further in view of *Nakagawa et al.*, U.S. Patent No. 5,650,834, *Hong et al.*, U.S. Patent No. 6,674,495, and *Kameyama et al.*, U.S. Patent No. 6,184,964.

Kim discloses [see Figs. 9-11 and 13A-13C] an array substrate for use in a liquid crystal display device, comprising a gate electrode [12], a gate line [11], and a gate pad electrode [13] on a substrate [100], wherein all of the gate electrode, the gate line, and the gate pad electrode have a double-layered structure including a first barrier metal layer [either Al-Nd or Cr] and an upper layer [either Mo or Al-Nd, respectively, see col. 6, lines 56-60], wherein the first barrier metal layer is interposed between the substrate and the upper layer; a gate insulating layer [20] on the substrate covering the double-layered gate electrode, gate line, and gate pad; an active layer [30] and an ohmic contact layer [40] sequentially formed on the gate insulation layer and over the gate electrode; a data line [51] on the gate insulating layer crossing the gate line, source and drain electrodes [52, 53] contacting the ohmic contact layer, and a data pad electrode on the gate insulating layer [see Fig. 13B]; a passivation layer [60] formed on the gate insulation layer to cover the data line, source and drain electrodes, and data pad electrode, wherein the passivation layer has a drain contact hole exposing the drain electrode, a gate pad contact hole exposing the gate pad electrode, and a data pad contact hole exposing the data pad [see Fig. 13C], and a pixel electrode [70], a gate pad terminal and a data pad terminal all of which are formed of a transparent conductive material on the passivation layer [see col. 7, lines 18-21].

Kim does not disclose that the gate wiring is double-layered with the upper layer being a first copper layer, or that all of the data line, the source and drain electrodes, and the data pad electrode have a double-layered structure including a second barrier metal layer and a second copper layer, wherein the second barrier metal layer is interposed between the substrate and the second copper layer, and wherein the first and second barrier metal layers include a metallic material that has a good adhesive characteristic to the substrate and prevents a reaction between the second copper layer and both the active layer and the ohmic contact layer.

Jo discloses an analogous device with double-layered gate and data wiring [Cu on Mo], with first and second barrier metal layers [Mo] and a first and second copper layer as recited [paragraph 0050, for instance]. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a [Mo-Cu] double-layers of *Jo* for the gate and data wirings in the device of *Kim*, motivated by *Jo's* teaching that the copper provides low resistance, low cost wiring [paragraph 0011] improving the display quality [paragraph 0006] and having a second barrier layer of Mo overcomes problems involved in forming the copper wiring [paragraphs 0012-0013,etc.]. The examiner notes that the metallic material is Mo, and it inherently has the recited adhesive and protective properties since it is the same material used by the applicant.

Kim also does not disclose that the gate wiring has a smooth taper shape without any steps on their sides. *Jo* does disclose this, as does *Onisawa* [see Fig. 1] which teaches that such gate lines should have a smooth taper rather than steps. It would have been obvious to one of ordinary skill in the art at the time of the invention to has

such a tapered shape in the device of *Kim*, motivated by *Onisawa*'s teaching that such a taper improves coverage of a film laminated thereon [col. 4, lines 9-12], for instance preventing breakage of the insulating film on the gate electrode and consequent short-circuits. Such a taper results in the sides of the first copper layer being inside of sides of the first barrier metal layer.

Kim also does not disclose a buffer layer between the substrate and the first barrier metal layer. *Terakado* discloses such a buffer layer [302], and it would have been obvious to one of ordinary skill in the art at the time of the invention to use such a barrier layer in the above device, motivated by *Terakado*'s teaching that this arrangement improves adhesion of the gate lines to the substrate [col. 10, lines 50-67].

Kim in view of *Jo* does not disclose that the metallic material is Ti or Ta; instead it uses Mo. However, this does not make the claims patentably distinct. First, *Jo* does in fact refer to using either Cu on Ti or Cu on Mo [see paragraph 0013]; although *Jo* then singles out Cu on Mo in particular, it is never made explicit why Mo is preferable to Ti, if indeed it is. Second, the prior art for such multi-layer electrodes evidences that these metals are art-recognized equivalents for the purpose. For instance, U.S. Patent No. 5,650,834 to *Nakagawa et al.* discloses the use of a double layer with Al, Ag, or Cu on top and Cr, Mo, Ta, W, or Ni on bottom [col. 4, lines 61-65, for instance]. U.S. Patent No. 6,674,495 to *Hong et al.* teaches using Al, Ag, or Cu for their low resistivity and Cr, Mo, or Ti for their good contact properties [col. 10, lines 20-24, for instance]. U.S. Patent No. 6,184,964 to *Kameyama et al.* teaches a triple-layer with the lowest layer Ti, Cr, Mo, W, Al, Ta, or Ni for their adhesion properties and the second layer Cu or Ag for

their low resistivity [see abstract, for instance]. From these prior art references, it can be seen that the use of Ta or Ti in place of Mo (as singled out by *Jo*, setting aside *Jo's* mentions of Ti), in a double layer electrode with Cu, would have been obvious to one of ordinary skill in the art as a matter of being art-recognized equivalents for the known purpose of providing good adhesion properties while the Cu layer provides low electrical resistance.

Claim 1 is therefore unpatentable.

The above references disclose the method of forming the above array substrate, as recited in claim 17, so claim 17 is also unpatentable.

Kim discloses [see Fig. 9] that the gate electrode extends from the gate line and the gate pad electrode is at an end of the gate line, so claims 2 and 18 are also unpatentable. The source electrode extends from the data line, and the drain electrode is spaced apart from the source electrode, and the data pad electrode is at an end of the data line, so claims 3 and 19 are also unpatentable. *Kim* discloses [either considering the drain contact hole to be the large opening in Fig. 13C, or more traditionally with reference to another embodiment, see Fig. 14, which can be equivalently used to reject claims 1 and 17] the pixel electrode disposed in a pixel region defined by the crossing of the gate and data line, wherein the pixel electrode contacts the drain electrode through the drain contact hole [see Fig. 13C, or element 56 in Fig. 14], wherein the gate pad terminal contacts the gate pad through the gate pad contact hole [14] and the data pad terminal contacts the data pad through the data pad contact hole [55], so claims 4 and 20 are also unpatentable. *Kim* discloses that the gate

insulation layer is an inorganic material selected from silicon nitride and silicon oxide [col. 4, lines 66-67], so claims 11 and 27 are also unpatentable. *Kim* discloses that the passivation layer can be made of silicon nitride [col. 5, lines 14-15], so claims 12 and 28 are also unpatentable.

Terakado's buffer layer is silicon nitride [col. 11, lines 12-17], so claims 14 and 30 are also unpatentable. The metallic material has good adhesive characteristic to the buffer layer, so claims 15 and 31 are also unpatentable.

4. Claims 9, 10, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Kim,* U.S. Patent No. 6,043,511 in view of *Jo et al.,* US 2002/0081847, in view of *Onisawa et al.,* U.S. Patent No. 5,739,877, in view of *Terakado et al.,* U.S. Patent No. 6,674,502, and further in view of *Nakagawa et al.,* U.S. Patent No. 5,650,834, *Hong et al.,* U.S. Patent No. 6,674,495, and *Kameyama et al.,* U.S. Patent No. 6,184,964 as applied above, and further in view of *Song,* U.S. Patent No. 6,091,464.

The above device does not disclose the storage capacitor recited in claims 9 and 25. *Song* does disclose a storage capacitor [see Figs. 4-5], comprising a portion of the gate line, a gate insulating layer as a dielectric layer, and a capacitor electrode which is formed simultaneously with the data lines, source and drain electrodes. It would have been obvious to one of ordinary skill in the art at the time of the invention to form such a capacitor in the above device, motivated by *Song's* teaching that this provides a good storage capacitance while preventing shorts between neighboring pixel electrodes [col. 5, lines 24-35, for instance]. When this capacitor is formed in the above device, the

capacitor electrode, made at the same time as the source/drain electrodes, will be double-layered, having the second barrier metal layer and the second copper layer. Claims 9 and 25 are therefore unpatentable. The double layer capacitor electrode would be connected in parallel with the pixel electrode through a contact hole [160] formed in the passivation layer, so claims 10 and 26 are also unpatentable.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andrew Schechter/
Primary Examiner, Art Unit 2871
Technology Center 2800
18 July 2008